ABSTRACT OF THE DISCLOSURE

An apparatus comprising an analysis block, a graphic user interface and a memory circuit. The analysis block may be configured to generate debug information in response to (i) a command input, (ii) one or more simulation outputs, and (iii) one or more compiler outputs. The graphic user interface may be configured (i) to present the command input in response to one or more user input parameters and (ii) to display the debug information. The memory circuit may be configured to store the one or more simulation outputs and said one or more compiler outputs.